Remarks

The instant Office Action dated September 18, 2009 notes the following rejections: claims 1, 5-8, 10, 20-23 and 27 stand rejected under 35 U.S.C. § 103(a) over Chudzik (U.S. Patent No. 7,030,481) in view of Dhong (U.S. Patent No. 6,221,769); claims 2-4 and 24-26 stand rejected under 35 U.S.C. § 103(a) over the '481 and '769 references and further in view of Hsuan (U.S. Patent Pub. 2001/0005046); and claim 9 stands rejected under 35 U.S.C. § 103(a) over the '481 and '769 references in view of Sakai (U.S. Patent No. 5,872,393). In this discussion set forth below, Applicant traverses all rejections and further does not acquiesce to any rejection or averment in the instant Office Action unless Applicant expressly indicates otherwise. Moreover, as the rejections are essentially repeated from the previous Office Action, Applicant fully incorporates its traversals of record herein.

The § 103(a) rejection of all claims cannot stand because the cited '481 reference, either alone or in combination with the '769 reference (or other references), lacks correspondence. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.*, a single layer of dielectric material that extends into both vertical capacitors and vias. In contrast, the Office Action acknowledges (at page 11) that the '481 reference does not specifically disclose a vertical trench capacitor and a vertical interconnect sharing a common dielectric material of "a single deposition layer". The '769 reference fails to overcome this lack of disclosure. While the Office Action has asserted that the '769 reference discloses a similar dielectric material (in referring to "Silicon Nitrate" rather than Silicon Nitride), nothing in the reference suggests that the via dielectric layer also acts as a dielectric for a trench capacitor (or any other device). As a further example, the '481 reference explicitly recites that its capacitor and via materials are different, explaining that the capacitor dielectric material is a "hi-K" material that requires special steps and tools that are incompatible with its interconnect layers. Therefore, the proposed combination fails to disclose, teach or suggest a common layer that includes both a capacitor dielectric and a via dielectric (the cited dielectric material in the '769 reference is exclusively used in vias), or that the vias in the '769 reference could or would be formed as asserted. All rejections thus fail.

Applicant further traverses the § 103 rejection of claims 1-10 and 20-27 because the cited references teach away from the Office Action's proposed combination. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('481) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). *See also In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984) (A §103 rejection cannot be maintained when the asserted modification undermines purpose of the main reference.).

In this instance, the teaching away in the '481 reference is evidenced in the reference itself, which explicitly teaches away from the combination with the '769 reference as asserted (to form a common dielectric layer). Specifically, the '481 reference acknowledges the method of manufacture of vertical interconnects described in the '769 reference (Col. 4:16-17), but requires that the corresponding dielectric layer be separate (and is formed in a separate, not common, step). The proposed combination and the disclosed approach in the '769 reference thus does not and cannot correspond to a single layer as claimed.

In addition, as the issues that the Office Action relies upon as alleged motivation are expressly addressed by the '481 reference, the asserted combination proposes a process that would not be implemented because it would both increase costs and attempt to implement an electronic device with improperly/unusable layers. The '481 reference explains that the material 3020 is a hi-K dielectric material (Col. 5:11-16) which requires special high temperature processing steps and tools to deposit it in the vertical trenches, which are incompatible with the conductors employed in the vias, and further explains that the hi-K material should be processed first in order to keep the costs at a minimum (Col. 5: 66 *et seq.*). Under M.P.E.P. § 2143.01 and the above-cited *KSR* and *In re Gordon* decisions, the rejections cannot be maintained.

Applicant also traverses each rejection because the Office Action's attempt to ignore limitations as "product by process" limitations is based upon a misapplication of

the law and an erroneous misreading of the claims, and further fails to establish correspondence to the ignored limitations. Specifically, the Office Action has improperly ignored various limitations based on an erroneous characterization of a single deposition layer limitation as a product by process step. Without acquiescing to the characterization of the "single deposition layer" as a product by process claim (and strongly traversing the same), Applicant respectfully reminds the examiner that under M.P.E.P. § 2113, when the structure implied by process steps would be expected to impart distinctive structural characteristics to the final product, the relevant limitations cannot be ignored. *See, e.g., In re Garnero*, 412 F.2d 276, 279 (CCPA 1979). As applied to these rejections, in each instance relevant distinctive structural characteristics would be present in the final product (*e.g.,* the commonality of the material, and the formation of the layered structures emanating from the same material and processing step(s) and tools); thus, the relevant limitations cannot be ignored.

Referring to the rejection of claim 23 as an example, the Office Action has improperly construed the limitation "a single deposition layer of dielectric material" as involving a process step. This erroneous interpretation is inconsistent with the claim, which is directed to a single layer of material "on the first and second sides of the substrate, on the conductive material lining each of the trenches, and on the walls of the vertical interconnect." That this layer was formed in a single deposition characterizes the layer, but does not permit the Examiner to ignore limitations directed to a single layer. The Office Action has not asserted that any reference discloses a single layer that includes both a trench capacitor insulator and a vertical interconnect insulator. Applicant has reviewed the cited references and cannot ascertain such a layer. Accordingly, by ignoring these limitations as process steps, the Office Action has failed to show correspondence to the claimed single layer.

In view of the above, neither reference teaches a single deposition layer of dielectric material in which the layer is used for both a via and vertical capacitor. Accordingly, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. The rejections therefore fail.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Juergen Krause-Polstorff, of NXP Corporation at (408) 474-9062.

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